# VLSI Neuroprocessors

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## Abstract

Electronic and optoelectronic hardware implementations of highly parallel computing architectures address several ill-defined and/or computation-intensive problems not easily solved by conventional computing techniques. The concurrent processing architectures developed are derived from a variety of advanced computing paradigms including neural network models, fuzzy logic, and cellular automata. Hardware implementation technologies range from state-of-the-art digital/analog custom-VLSI to advanced optoelectronic devices such as computer-generated holograms and e-beam fabricated Dammann gratings. JPL's Concurrent Processing Devices Group has developed a broad technology base in hardware implementable parallel algorithms, low-power and high-speed VLSI designs and building block VLSI chips, leading to application-specific high-performance embeddable processors. Application areas include high throughput map-data classification using feedforward neural networks, terrain based tactical movement planner using cellular automata, resource optimization (weapon-target assignment) using a multidimensional feedback network with lateral inhibition, and classification of rocks using an inner-product scheme on Thematic Mapper data. In addition to addressing specific functional needs of DoD and NASA, the JPL-developed concurrent processing device technology is also being customized for a variety of commercial applications (in collaboration with industrial partners), and is being transferred to U.S. industries.

This talk will focus on two application-specific processors which solve the computation intensive tasks of resource allocation (weapon-target assignment) and terrain based tactical movement planning using two extremely different topologies. Resource allocation is implemented as an asynchronous analog competitive assignment architecture inspired by the Hopfield network. Hardware realization leads to a two to four order of magnitude speed-up over conventional techniques and enables multiple assignments, (many to many), not achievable with standard statistical approaches. Tactical movement planning (finding the best path from A to B) is accomplished with a digital two-dimensional concurrent processor array. By exploiting the natural parallel decomposition of the problem in silicon, a four order of magnitude speed-up over optimized software approaches has been demonstrated.

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## Neural Networks–Cartographic Applications Group

Efforts of the JPL Cartographic Applications Group

### Neural Nets & Map Separation

- Extract Roads, Rivers, Urban Areas, etc. out of digitally scanned paper maps & CD-ROM data using trained neural networks. (N. Ritter)

### Neural Nets & Multispectral Classification

- Prepare ground-use info and detect man-made features & land-types from hyperspectral airborne AVIRIS data, trained neural networks and ground truth. (N. Ritter)

### Concurrent Processing Applications

- TMA: Tactical Movement Analysis finds optimal path over varied terrain using concurrent processing with transputer arrays (T. Kreitzberg)

- LOS: Line of sight computations using tiled data-decomposition with transputers. (T. Kreitzberg)

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# Concurrent Processing Devices Group

- Electronic and Optoelectronic Hardware Implementations of Highly Parallel, Neural Network-Inspired Computing Architectures
  - Neurocircuit Simulations of Parallel Architectures
  - Research on Novel Computing and Memory Devices
    amorphous semiconductors, composite oxides, and ferroelectric materials
  - Hardware Implementations of Custom VLSI ICs that can be Embedded into Neuroprocessor Cards

Flexible General purpose Building Block Chips
- Cartographic analysis
- Adaptive Controller for Interceptor
- Space Environmental Test

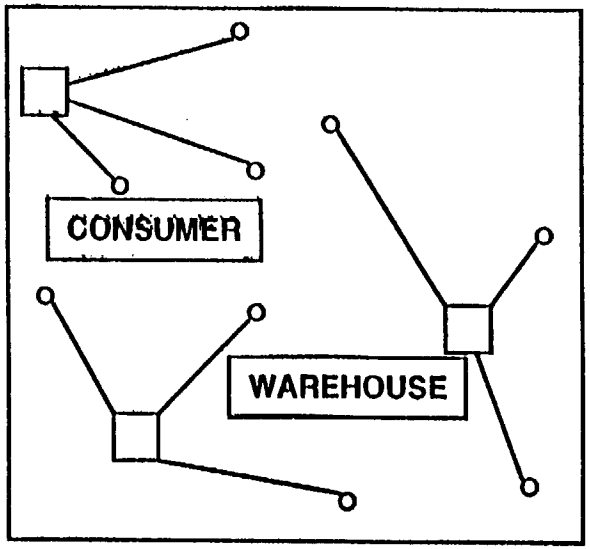
Application Specific ICs
- Resource Allocation
- Path Planning
- Image Compression

- Technology Transfer to U.S. Industry Ongoing
- Development over the Past 8 Years Sponsored By: NASA, BMDO/IST, ARPA, CECOM/IEWD, ONR, NSWC, NAWC, CSDL, USA/SSDC, AFOSR, and Industry

# RESOURCE ALLOCATION / ASSET MANAGEMENT

- ***DEVELOPED A NEW BREAKTHROUGH CONCEPT FOR HARDWARE IMPLEMENTATION OF A NEUROPROCESSOR FOR HIGH SPEED SOLUTIONS TO DYNAMIC ASSIGNMENT PROBLEMS.***

- RESOURCE ALLOCATION
- DYNAMIC ASSIGNMENT
- MESSAGE ROUTING
- TARGET-WEAPON PAIRING
- LOAD BALANCING
- MULTI-TARGET TRACKING
- SEQUENCING / SCHEDULING
- ASSET MANAGEMENT
- REAL-TIME, ADAPTIVE MISSION RE-PLANNING



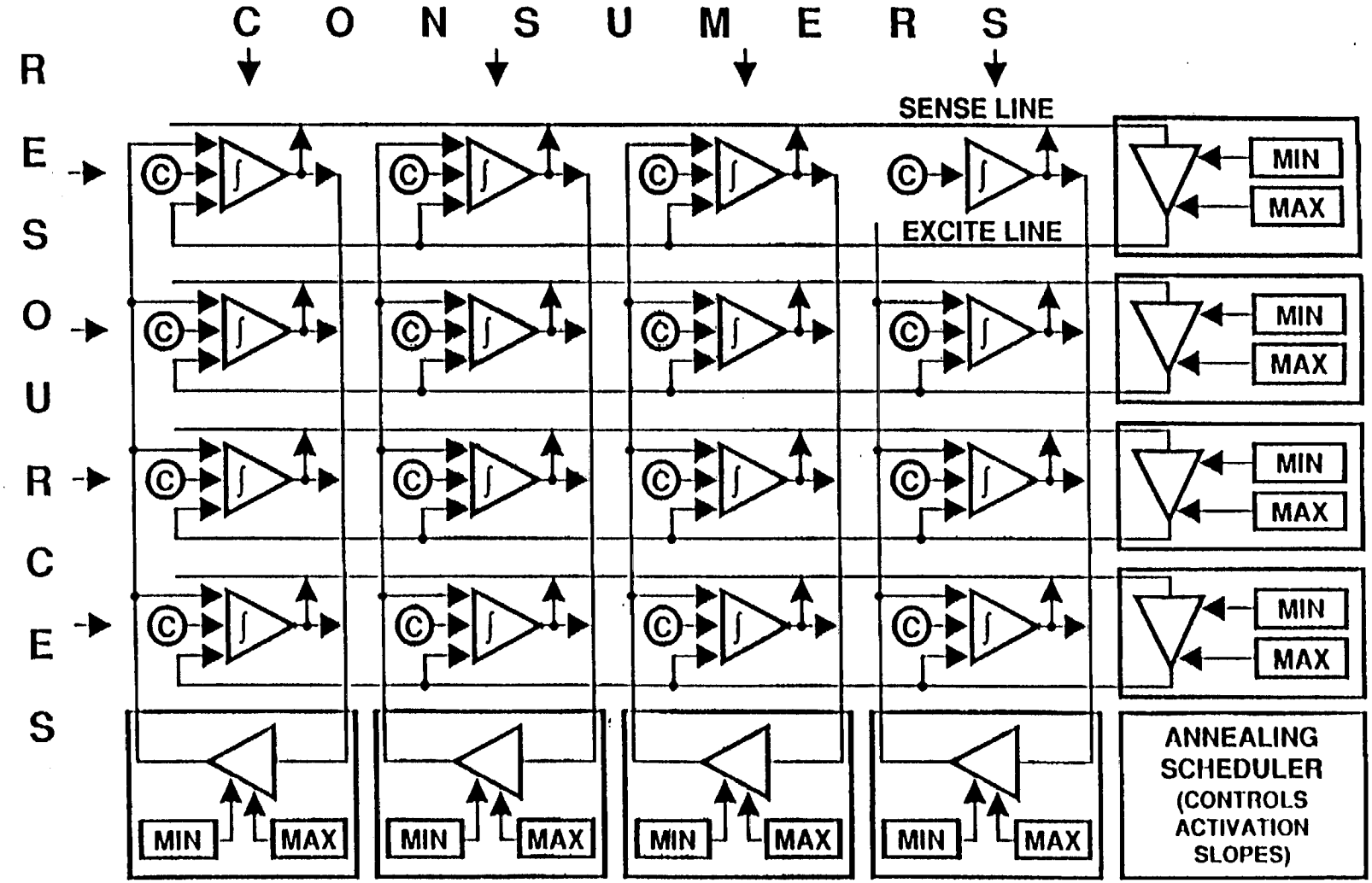

3 WAREHOUSES AND 9 CONSUMERS

ASSIGN

3 CONSUMERS TO EACH WAREHOUSE TO OBTAIN MINIMUM OVERALL COST

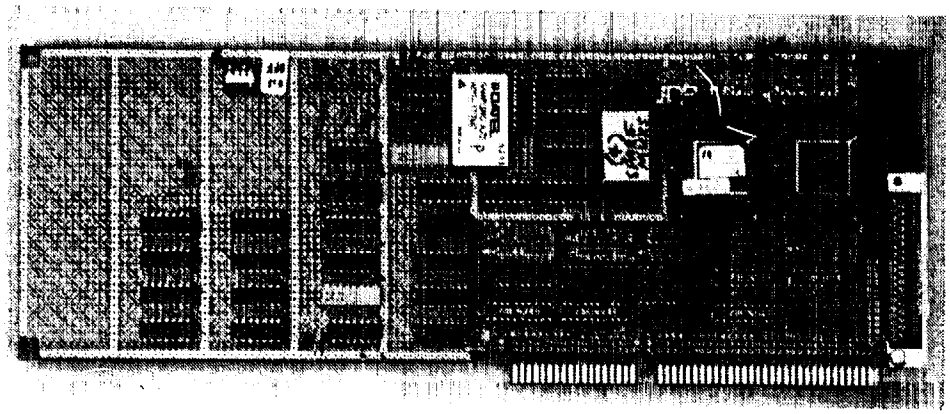
- ***NEUROPROCESSING APPROACH OFFERS OVER 4 ORDERS OF MAGNITUDE SPEED ENHANCEMENT OVER CONVENTIONAL COMPUTING TECHNIQUES.***
- ***ARBITRARY MULTIPLE (MANY - TO - MANY) ASSIGNMENTS ARE MADE, WHICH ARE NOT EASILY ACCOMPLISHED BY CONVENTIONAL TECHNIQUES.***

# Asset Management Neuroprocessor IC Architecture

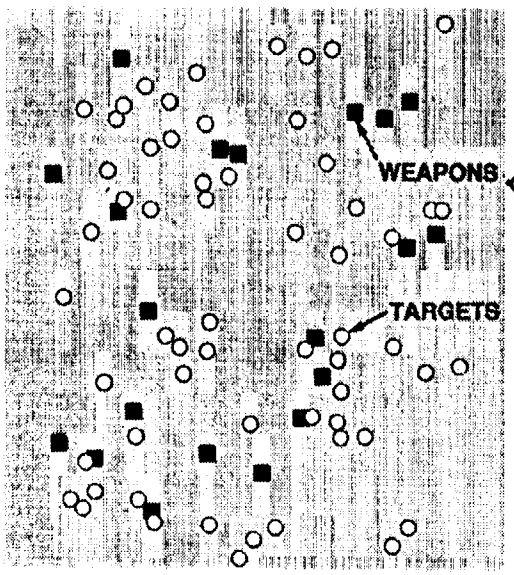


# NEUROPROCESSOR FOR WEAPON-TARGET ASSIGNMENT

## PLUG-IN NEUROPROCESSOR CARD

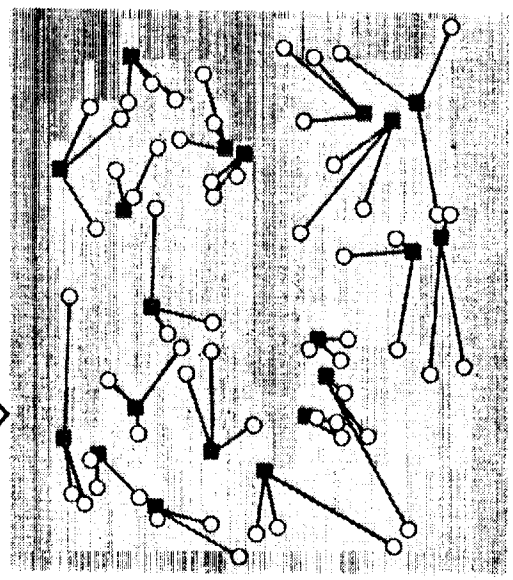


- FULLY PARALLEL ARCHITECTURE OF NEURAL NET HARDWARE PERFORMS DYNAMIC ASSIGNMENT OF RESOURCES
- NEUROPROCESSING SPEED SURPASSES THAT OF AN 8-NODE HYPER-CUBE BY TWO ORDERS OF MAGNITUDE
- A 40X40 ASSIGNMENT CHIP WITH 1600 ANALOG NEURONS GIVES A "GOOD" SOLUTION OUT OF A TOTAL OF OVER $10^{48}$ POSSIBLE COMBINATIONS
- FOR THE FIRST TIME IT ENABLES MANY-TO-MANY ASSIGNMENTS




A 60 TARGETS TO 20 WEAPONS (3-TO-1) ASSIGNMENT

SIMULATION OF HARDWARE PROMISES ASSIGNMENT IN ABOUT 30 MICROSECONDS



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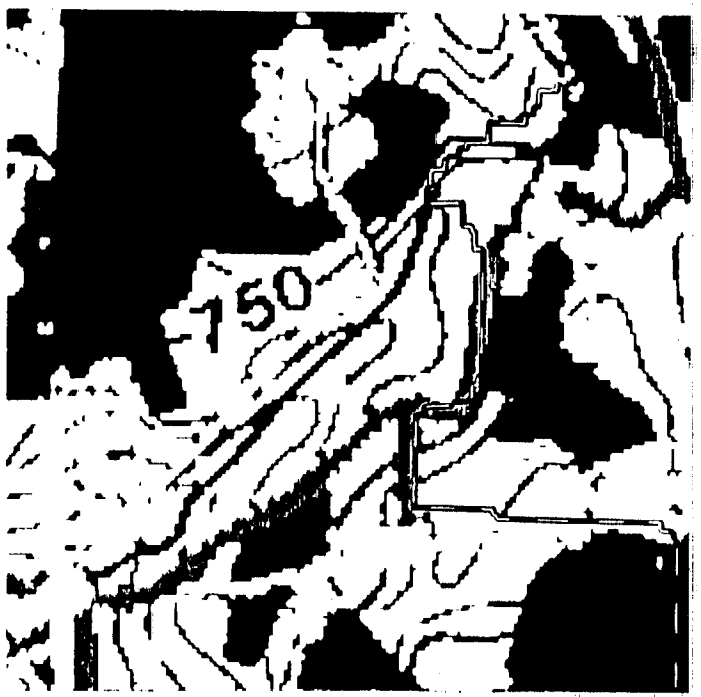
# PATH PLANNING

**OBJECTIVE:** TO FIND LEAST COST (MINIMIZING TIME, FUEL, ATTRITION, ETC.) PATH ACROSS COMPLEX TERRAIN QUICKLY (ms)




## APPLICATION AREAS

- DEFENSE
  - TACTICAL MOBILITY ANALYSIS FOR BATTLEFIELD SCENARIOS
  - MISSION PLANNING: REAL TIME ROUTE PLANNING AND EN ROUTE RE-ROUTING FOR FLIGHT PLATFORMS
- EMERGENCY DISPATCHING (CIVILIAN AND MILITARY)
- AUTONOMOUS VEHICLE NAVIGATION
- CIRCUIT BOARD WIRE ROUTING/MAZE NAVIGATION

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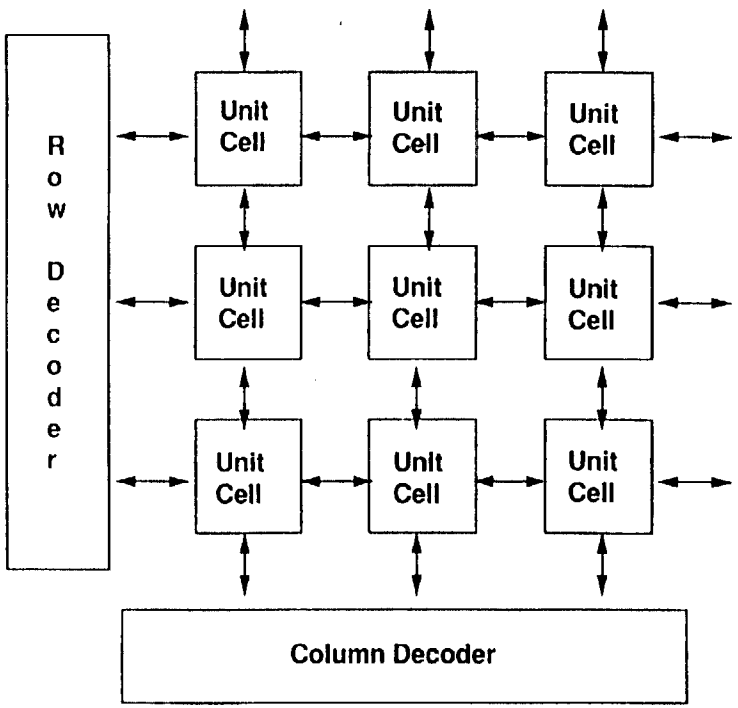
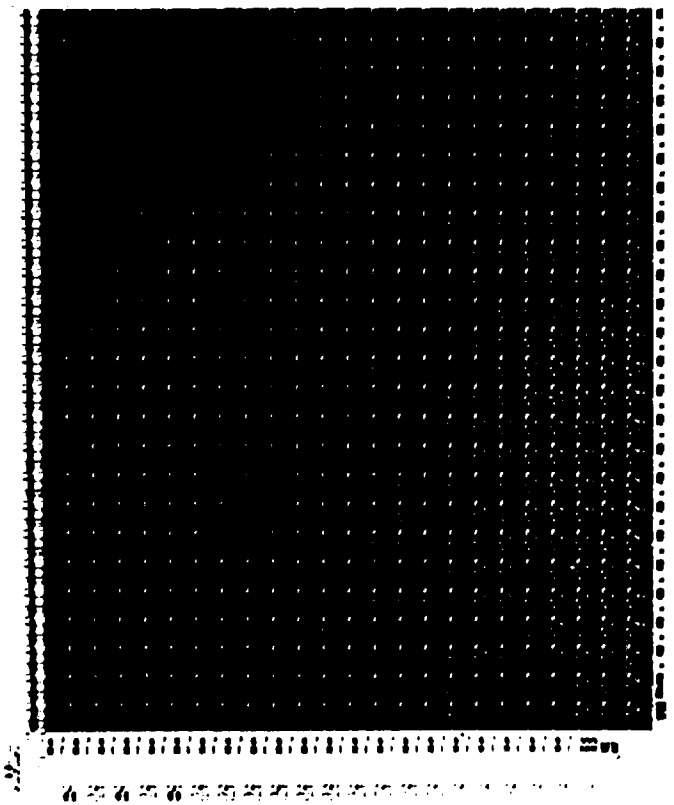
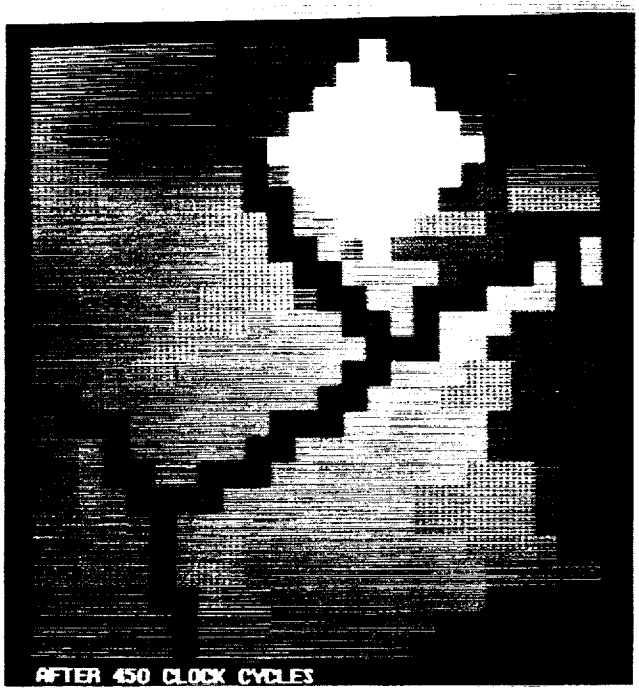
# PATH PLANNING APPROACH

**PROBLEM:** CURRENT SOFTWARE APPROACHES REQUIRE SECONDS TO MINUTES TO COMPUTE LEAST COST PATH

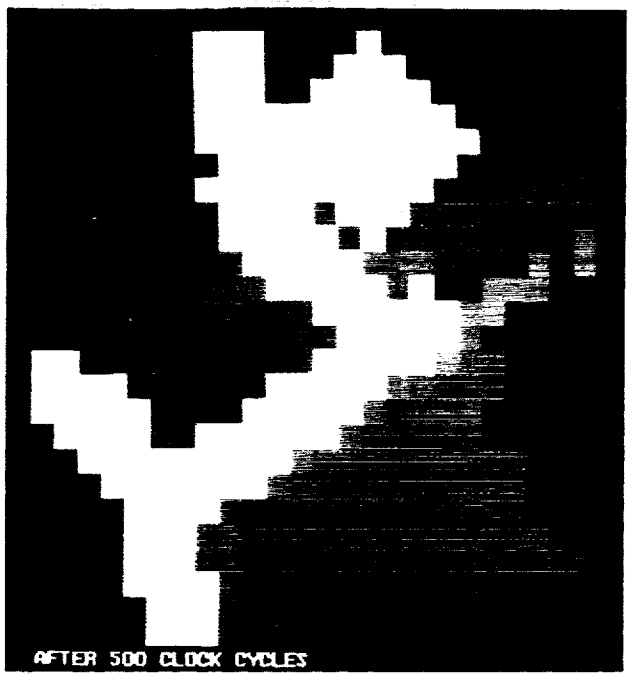
**SOLUTION:** VLSI INTEGRATION OF A FINE GRAIN PARALLEL PROCESSOR ARRAY PROGRAMMED TO MODEL A GIVEN TERRAIN AND DETERMINE THE LEAST COST PATH IN MILLISECONDS



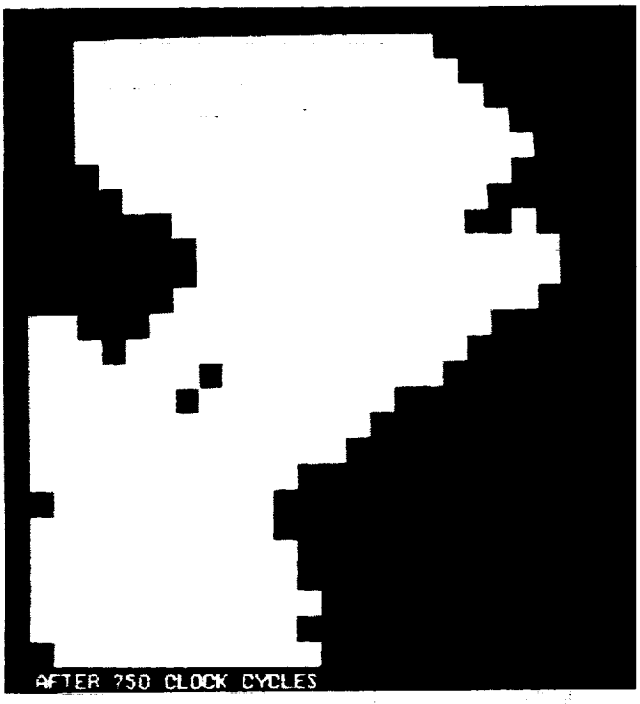





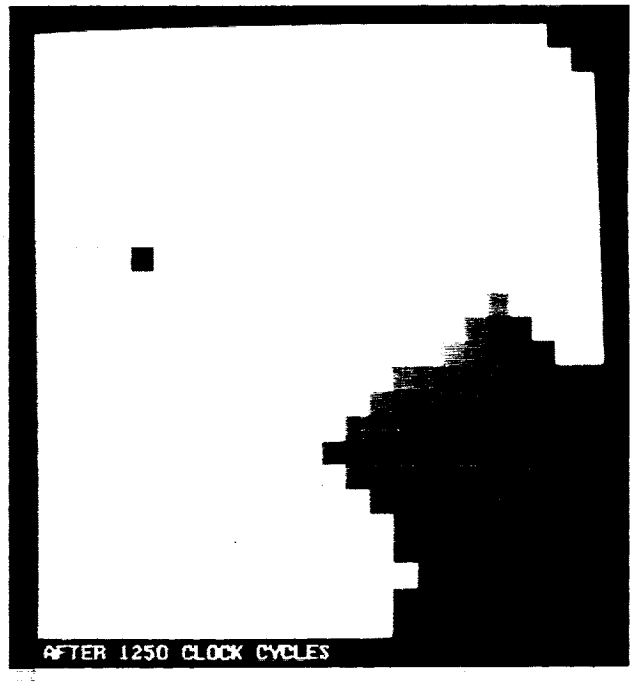

(a)




(b)




(c)

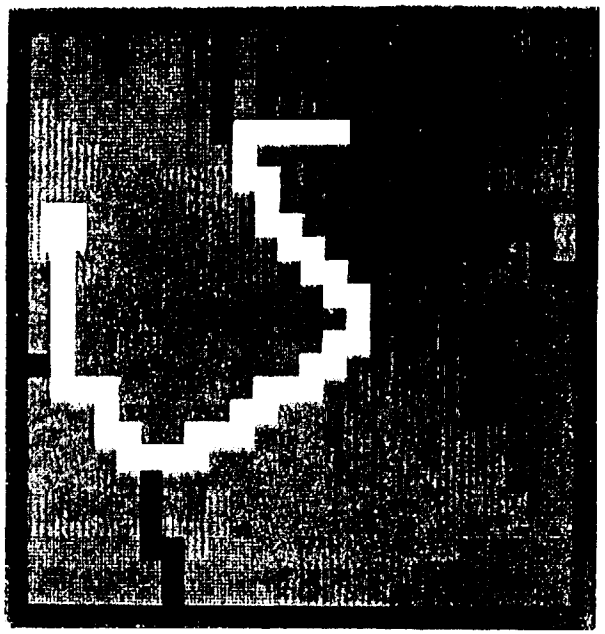



(d)

Signal propagation through array shown in white on map background (black indicates road): a) after 450 clock cycles, b) after 500 clock cycles, c) after 750 clock cycles, and d) after 1250 clock cycles.

# JPL PATH PLANNER PERFORMANCE SUMMARY

## TYPICAL LEAST COST PATH



## IC CHARACTERISTICS

| | |
|---|---|
| CHIP ARCHITECTURE: | 24 x 25 DIGITAL PROCESSOR ARRAY |
| MAXIMUM CLOCK FREQUENCY: | 7 MHz |
| EQUIVALENT OPERATIONS PER SECOND: | 6 BILLION |
| ORIGINATION NODES: | ONE OR MULTIPLE |
| COST DYNAMIC RANGE: | 256:1 |
| PROCESS: | 2 μm CMOS |
| UNIT CELL (PROCESSOR) SIZE: | 296 μm x 330 μm |
| IC SIZE: | 7.9 mm x 9.2 mm |

## AVERAGE PATH DETERMINATION SPEEDS

| TERRAIN GRID DIMENSION | CURRENT SOFTWARE ($N^2$ ALGORITHM, 4 TRANSPUTERS) | PATH PLANNER IC (7 MHz CLOCK) |
|---|---|---|
| 24 x 25 | — | 0.23 ms |
| 64 x 64 | 4 sec | 0.58 ms |
| 128 x 128 | 17 sec | 1.17 ms |
| 256 x 256 | 74 sec | 2.34 ms |
| 512 x 512 | 320 sec | 4.68 ms |

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Path Planning

# SUN Software Simulation

- Ported Vector-Cost Path Planner Software to SUN (programmable cost for each of 8 directions)
  - **Portable** - will run on any workstation that supports UNIX, Xwindows, and Motif
  - **Modular** - can easily replace software modules with hardware
  - **Friendly Graphics Interface** pushbuttons, pop-up menus, scroll bars

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# CONCLUSIONS

- **Neural Networks have Matured, Enabling Solutions to a Variety of Ill-Defined, and/or Computation-Intensive Problems**
- **Ongoing Technology Insertion Strategies**
  - **Embeddable NN Hardware (User Transparent, Inexpensive)**
    - » **PC Co-Processor Boards**
    - » **Small Stand-Alone Packages (e.g. automotive "under the hood", medical devices)**
- **Further Developments in Novel Architectures will Lead to Enabling New Capabilities**
    - » **3-D ULSI/Optoelectronic Implementations**